



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No. : 10/691,080 **Confirmation No.:** 9280

Applicants: Barry E. Burke et al.

Filed: October 22, 2003

TC/A.U.: 2818

Examiner: C. Luu

Docket No.: MIT8431L

For: High-Yield, Single-Level Gate Charge-Coupled
Device Design and Fabrication

COMMISSIONER FOR PATENTS
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ALEXANDRIA, VIRGINIA 22313-1450

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August 10, 2005
[Signature]

INFORMATION DISCLOSURE STATEMENT FILED PURSUANT
TO THE DUTY OF DISCLOSURE UNDER 37 CFR §1.56, §1.97, AND §1.98

Pursuant to the duty of disclosure under 37 CFR §1.56, §1.97, and §1.98, the Applicants
request consideration of this Information Disclosure Statement.

Compliance with 37 CFR §1.97:

This Information Disclosure Statement is hereby filed under §1.97 (c) at a time prior to
the mailing date of a final action or notice of allowance.

Please apply the fee amount of \$180.00 under 1.17(p) to Deposit Account No. 19-2553.
If any other fees are required, or there are any credits, please also apply such to Deposit Account
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Information Cited:

The Applicants hereby make of record in the instant application the information listed on the attached two (2) pages of Forms PTO/SB/08A and PTO/SB/08B. The order of presentation of the references on the forms should not be construed as an indication of the importance of the references. A copy of each of the listed items is enclosed.

Remarks:

The Applicants respectfully request that:

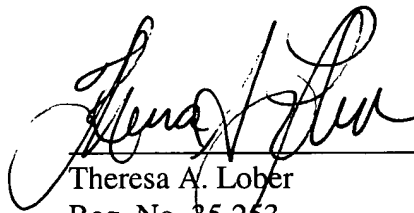
1. The Examiner consider completely the cited information in reaching a determination concerning the patentability of the pending claims;
2. The enclosed two (2) pages of Forms PTO/SB/08A and PTO/SB/08B be initialed and signed by the Examiner and a signed copy returned to the undersigned Agent to evidence that the cited information has been fully considered by the Patent and Trademark Office during the examination of this application; and
3. The citations for the information listed on the enclosed two (2) pages of Forms PTO/SB/08A and PTO/SB/08B be printed on any patent which issues from this application.

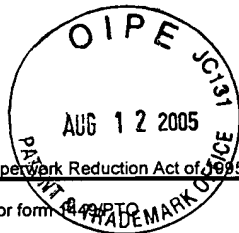
In submitting this Information Disclosure Statement, the Applicants make no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist. In submitting this Information Disclosure Statement, the Applicants make no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 CFR §1.56(b). In submitting this Information Disclosure Statement, the Applicants make no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. §102.

Notwithstanding any statements by the Applicants, the Examiner is urged to form his own conclusion regarding the relevance of the cited information. An early and favorably action is hereby requested.

Respectfully Submitted

Date: August 10, 2005
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Facsimile: 978.369.7101


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PTO/SB/08A (07-05)

Approved for use through 07/31/2006. OMB 0651-0031
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Substitute for form 1449 PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	10/691,080
Filing Date	October 22, 2003
First Named Inventor	Barry E. Burke
Art Unit	2818
Examiner Name	C. Luu
Attorney Docket Number	MIT8431L

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	A1	US- 3,728,590	04-17-1973	Kim et al.	
	A2	US- 3,853,634	12-10-1974	Amelio et al.	
	A3	US- 5,298,448	03-29-1994	Stevens et al.	
	A4	US- 4,063,992	12-20-1977	Hosack	
	A5	US- 4,613,402	09-23-1986	Losee et al.	
	A6	US- 5,302,544	04-12-1994	Lavine	
	A7	US- 5,314,836	05-24-1994	Lavine	
	A8	US- 5,556,801	09-17-1996	Hawkins et al.	
	A9	US- 5,606,187	02-25-1997	Bluzer et al.	
	A10	US- 5,719,075	02-17-1998	Hawkins et al.	
	A11	US- 5,760,431	06-02-1998	Savoye et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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		Examiner Name	C. Luu		
Sheet	2	of	2	Attorney Docket Number	MIT8431L

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	B1	BROWNE et al., "A Nonoverlapping Gate Charge-Coupling Technology for Serial Memory and Signal Processing Applications," IEEE Jnl of Solid-State Circuits, Vol. SC11, No. 1, pp. 203-207, February 1976.	
	B2	KAPOOR, "Charge-Coupled Devices with Submicron Gaps," IEEE Electron Device Ltrs., Vol. EDL-2, No. 4, pp. 92-94, April 1981.	
	B3	SLOTBOOM et al., "Submicron CCD memory structures fabricated by electron-beam lithography," Proc. IEDM '84, paper 11.6, pp. 308-311, 1984.	
	B4	GAJAR et al., "An ionic liquid-channel field-effect transistor," J. Electrochem. Soc., V. 139, No. 10, pp. 2833-2840, October 1992.	
	B5	YAMADA et al., "Driving Voltage Reduction in a Two-Phase CCD by Suppression of Potential Pockets in Inter-Electrode Gaps," IEEE Trans. on Electron Devices, V. 44, No. 10, pp. 1580-1587, October 1997.	
	B6	OKADA et al., "Performance of FT-CCD image sensor with Single Layer Poly-Silicon Electrode," 1999 IEEE Workshop on Charge-Coupled Devices and Advanced Imager Sensors, pp. 219-222, Nagano, Japan, June 1999.	
	B7	BURKE et al., "Charge-coupled device made with a single polysilicon level," Massachusetts Institute of Technology Lincoln Laboratory Solid State Research Quarterly Technical Report, pp. 31-37, March 1, 2002.	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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